WHAT IS CLAIMED IS:

1. A routing method for a multiplex system having N inputs each designed to receive one of N input multiplexes each having M input channels, each of the channels serving to transport an input packet, and N' outputs each serving to generate one of the N' output multiplexes each made up of output channels each serving to transport an output packet, each of the M channels used in the input multiplex comprising a data packet associated with an input header serving firstly to identify the packet and secondly to specify at least one output to which it is to be routed, wherein each of the N' output multiplexes has M+L channels with $L \geq 0$, and wherein the method implements the following operations:

· for the data, multiplexing N input channels each having M multiplexed packets so as to generate an aggregate multiplex signal comprising all of the data packets representing the N input multiplexes; and

· for each of the N' outputs, providing the inputs of M+L selection chains disposed in parallel with access to the aggregate multiplexed signal;

· for the input headers, performing demodulation and decoding;

· for the output headers, performing encoding and modulation on the basis of the demodulated and decoded input headers; and

· for the headers and the data, selecting from n of the M+L selection chains corresponding to the k^{th} output on the basis of the input headers corresponding to n packets that are to be routed to the k^{th} of the N' outputs, the corresponding n data packets in the aggregate multiplexed signal and multiplexing these n data packets with the corresponding n output headers in order to generate the k^{th} output multiplex, where k = 1, 2, ..., N'.

2. A method according to claim 1, wherein L is a non-zero integer.

3. A method according to claim 1, wherein each of the input multiplexes comprises data packets and a signalling channel containing headers,

and wherein each of the N input multiplexes is demultiplexed in order to separate the headers from the data packets.

4. A method according to claim 1, wherein said selection comprises:

· preliminary selection to select from the aggregate multiplexed signal the input multiplex(es) containing the data packets to be routed to the k^{th} output; and

· packet selection to select from each of said input multiplexes the data packet(s) to be routed to the k^{th} output.

5. A method according to claim 1, wherein the aggregate multiplexed signal is generated by code- or frequency- or wavelength-division multiplexing for the N input multiplexes, a said code, frequency, or wavelength being allocated to each input multiplex, and wherein said preliminary selection implements demultiplexing using said code or frequency or wavelength.

6. A method according to claim 4, wherein the aggregate multiplexed signal is generated by code- or frequency- or wavelength-division multiplexing for the N input multiplexes, a said code, frequency, or wavelength being allocated to each input multiplex, and wherein said selection implements first code- or frequency- or wavelength-division demultiplexing to perform the preliminary selection, and second code- or frequency- or wavelength-demultiplexing to perform said packet selection.

7. A method according to claim 1, wherein said multiplexing of the selected data packets implements:

· code- or frequency- or wavelength-division multiplexing of the data packets to be routed to the k^{th} output; and

· code- or frequency- or wavelength-division multiplexing of the headers corresponding to said data packets to be routed to the k^{th} output.

8. A method according to claim 7, wherein the selected data packets and headers are multiplexed in the output multiplex of the k^{th} output.

9. A device for implementing the method according to claim 1, the device presenting:

· a first system comprising:

· an N input multiplexing module for receiving and multiplexing the N input multiplexes, each of which comprises up to M multiplexed packets, and for generating as output said aggregate multiplexed signal;

· a distributor circuit such as a bus for distributing said aggregate multiplexed signal to an input of each of N' processing chains each allocated to one of the N' outputs of the device and each presenting M+L selection circuits in parallel; and

· each selection circuit presenting in series a beam selector, a channel selector, and a channel converter; and

· a second system comprising:

· a demodulation and decoding circuit presenting N inputs for receiving the headers corresponding to the data packets in each of the N input multiplexes and for demodulating and decoding said headers;

· a processor circuit for processing the demodulated and decoded input headers to configure the

beam selector and the channel selector in at least some of the M+L selection circuits in each of the processing chain so that each said selection circuit selects a packet for routing to the output with which it is associated:

· a header generator module for generating, for each output, the output headers corresponding to each of the n output data packets from said selection circuits of said output; and

· an encoder and modulator circuit for encoding and modulating the output headers generated by the header generator module;

and wherein, for each of said selection circuits, the channel converter presents means for adding to each of said data packets an output channel identification signal so as to place said n data packets belonging to the same output on different channels;

and wherein the device includes an output multiplexer module for each of said N' outputs of the device to multiplex the data packets allocated to said outputs with the output headers corresponding to said packets.